

FIG. 1(A)

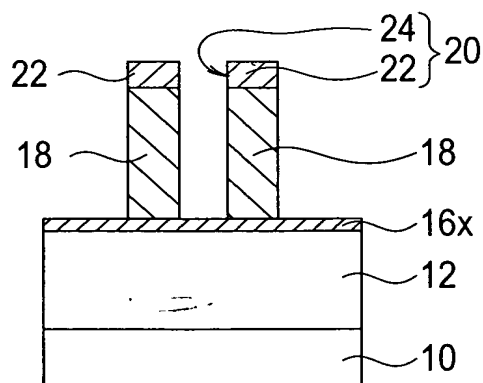


FIG. 1(B)

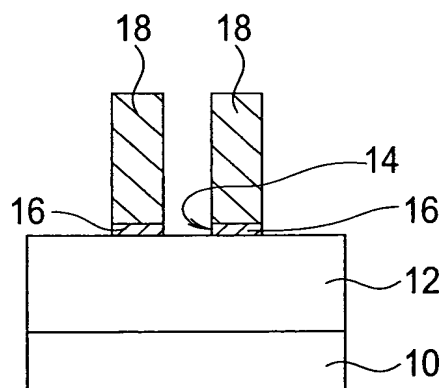
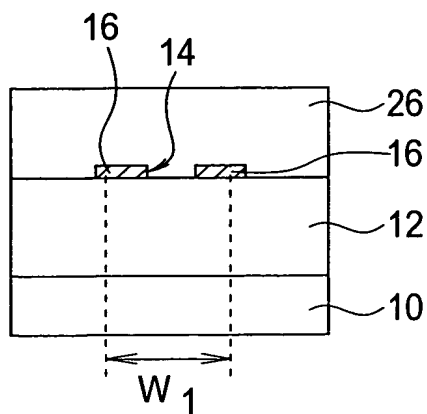
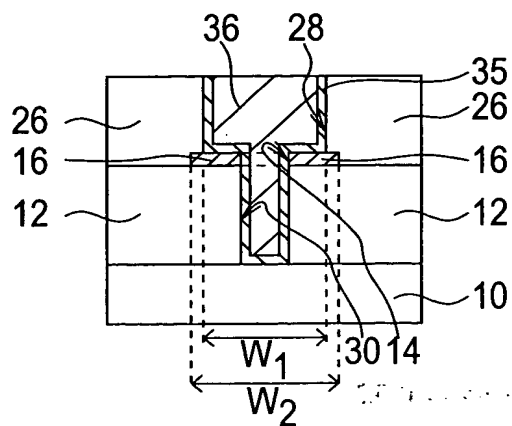


FIG. 1(C)





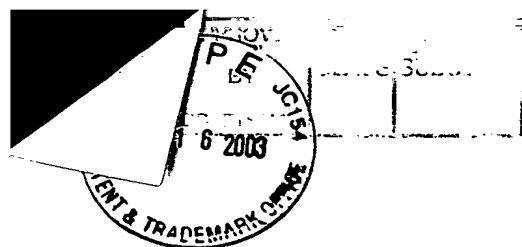


FIG. 3(A)

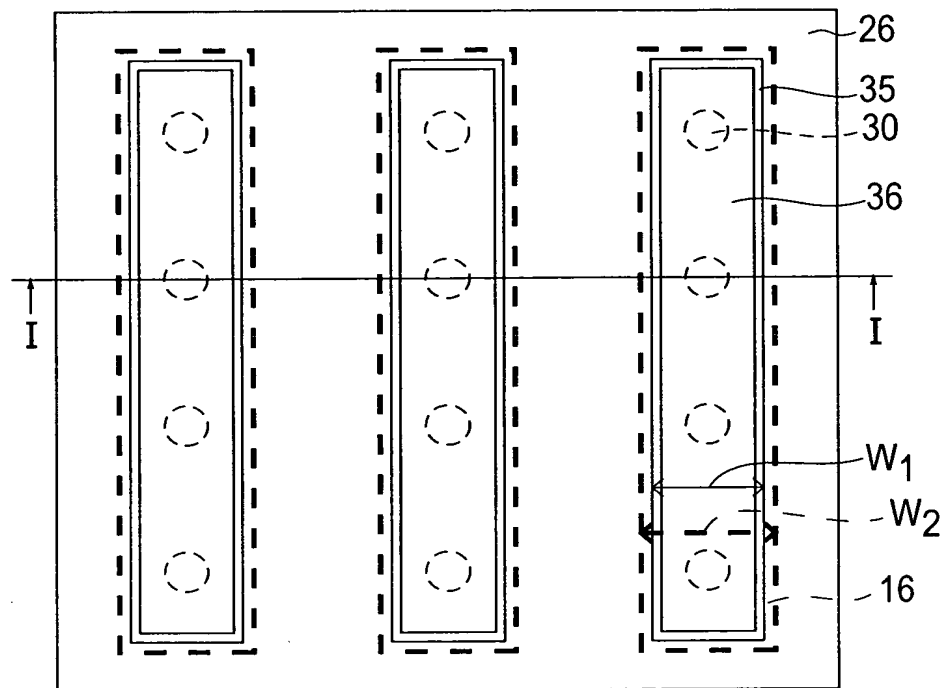
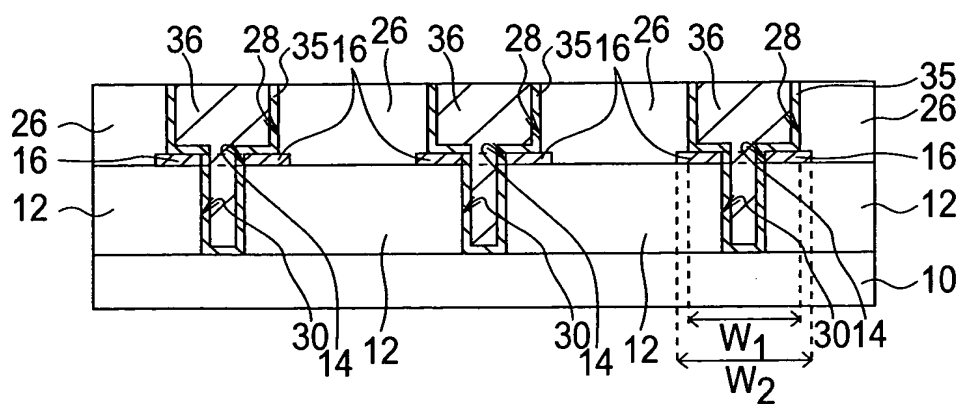


FIG. 3(B)



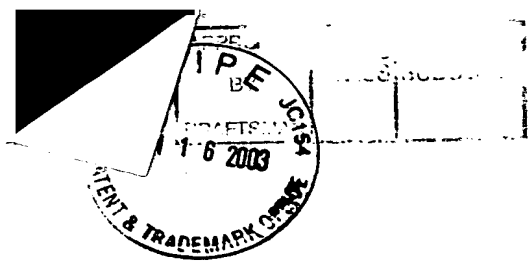
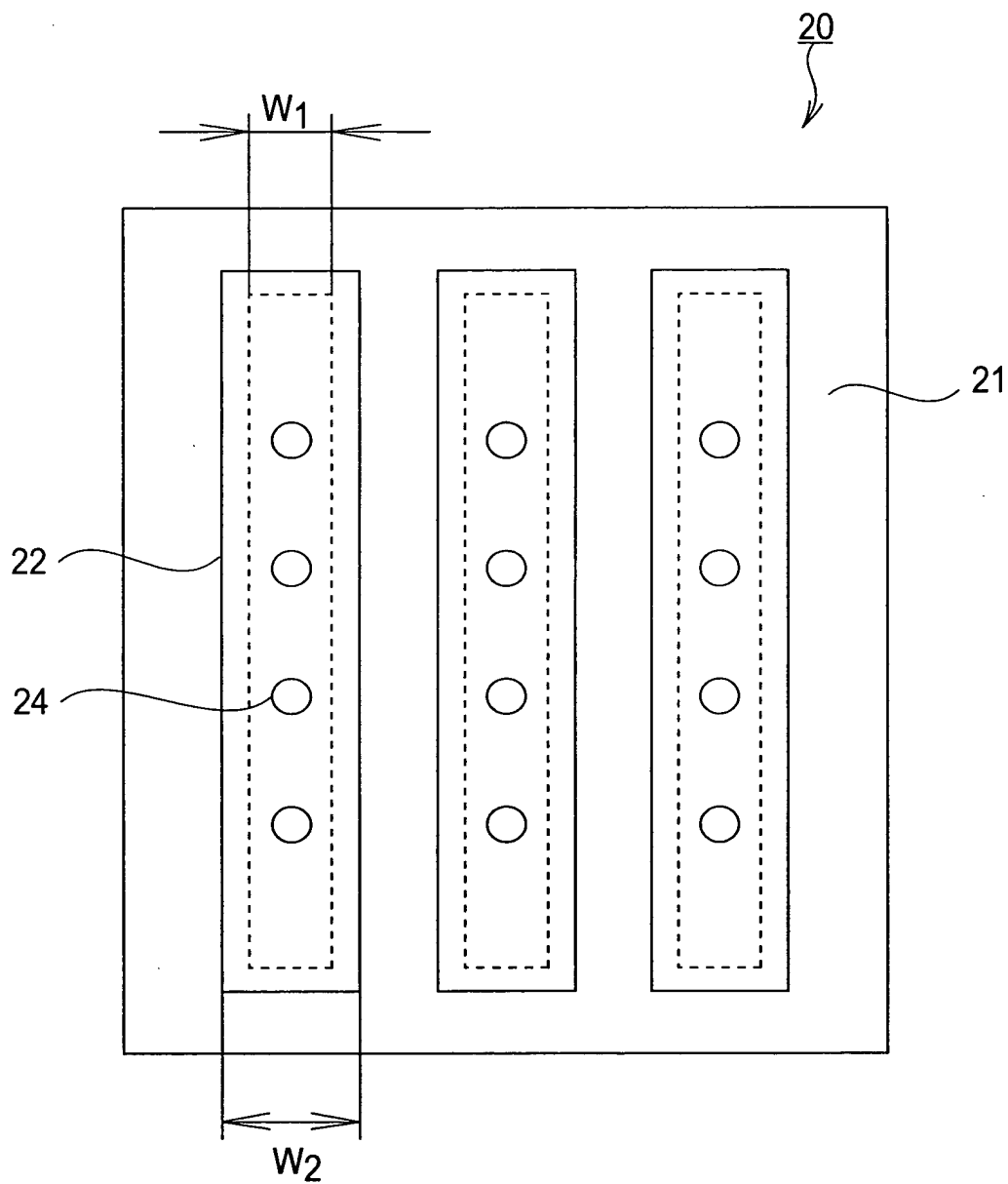


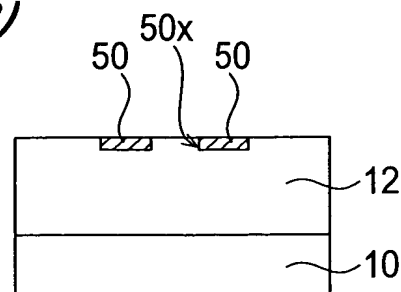
FIG. 4

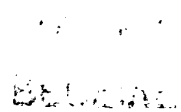


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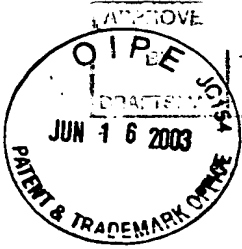


FIG. 7(A)

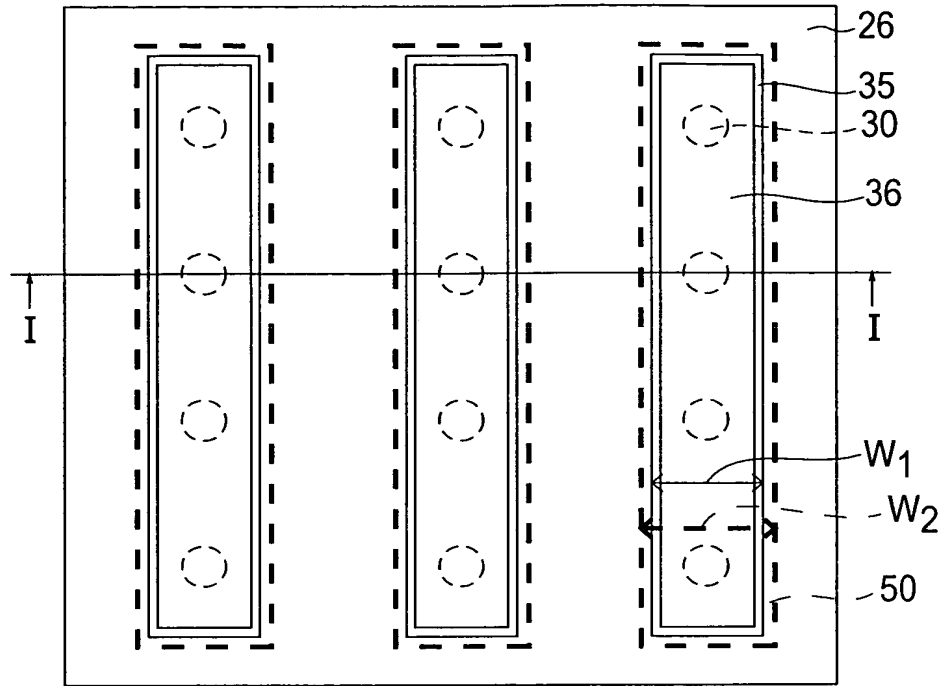


FIG. 7(B)

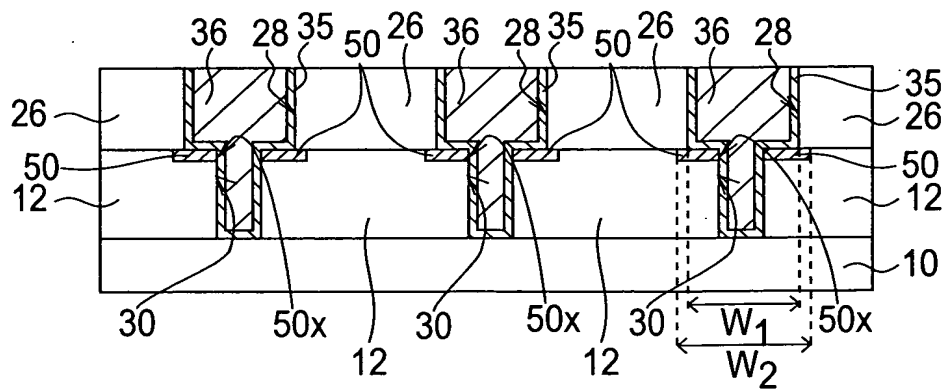


FIGURE 7 - OTHER SHEL

FIGURE 7

FIGURE 7



FIG. 8(A)

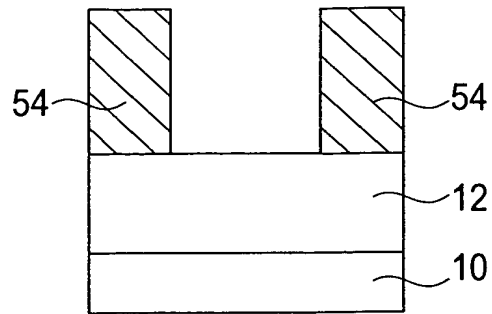


FIG. 8(B)

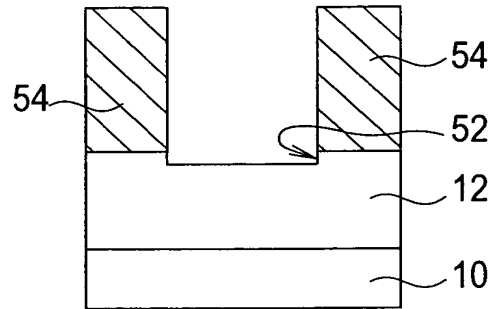


FIG. 8(C)

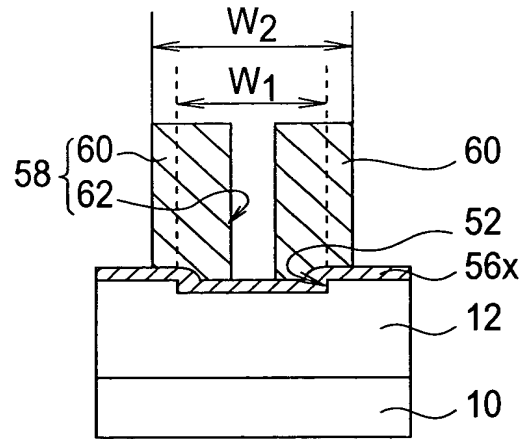
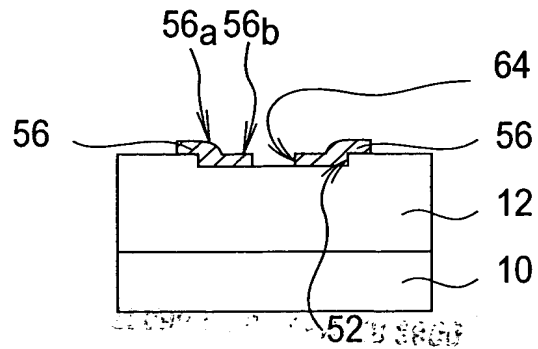


FIG. 8(D)



A cross-sectional view of a semiconductor device. It shows a substrate 10 with a trench 12. A layer 52 is formed on the bottom of the trench 12. A layer 56 is formed on the side walls of the trench 12. A layer 26 is formed on the top surface of the substrate 10. A layer 36 is formed on the top surface of the substrate 10, and a layer 28 is formed on the top surface of the substrate 10. A layer 35 is formed on the top surface of the substrate 10. The width of the trench 12 is indicated by W_1 and W_2 . A dimension 30 is also indicated.



FIG. 10(A)

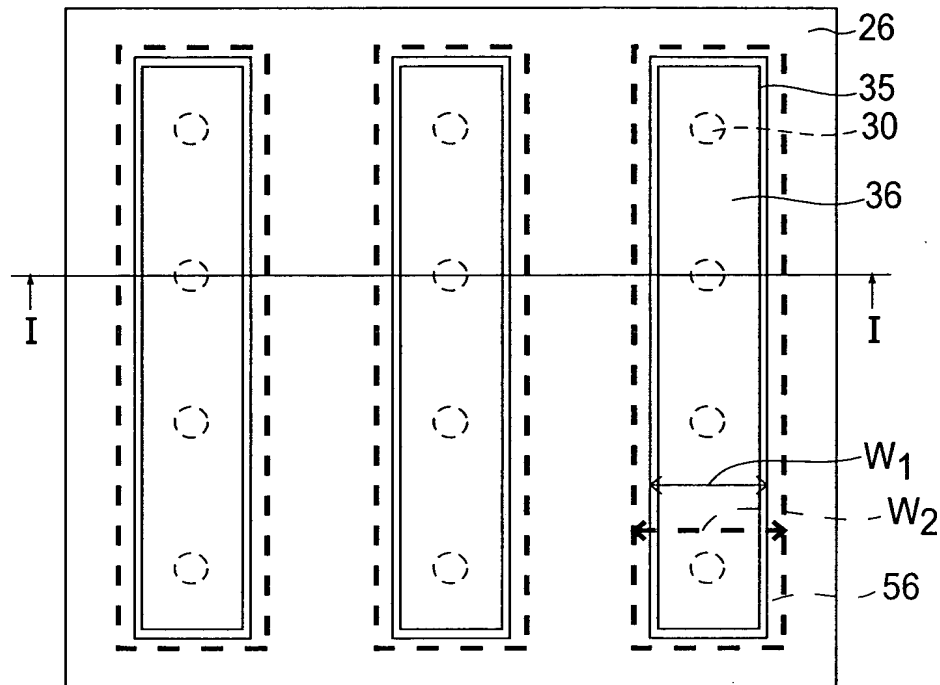
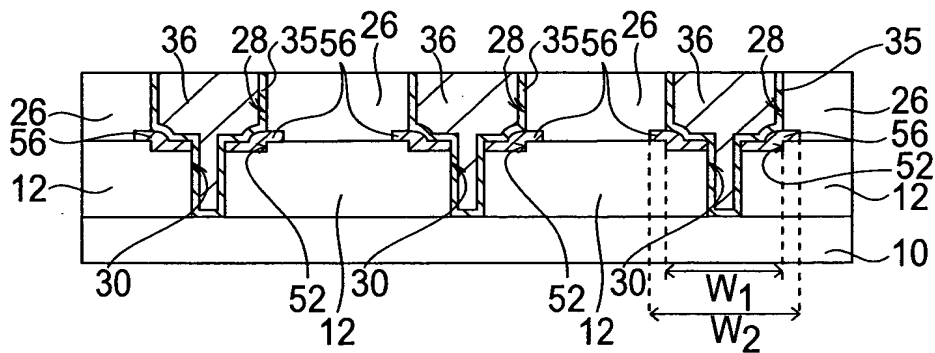


FIG. 10(B)



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FIG. 11(A)

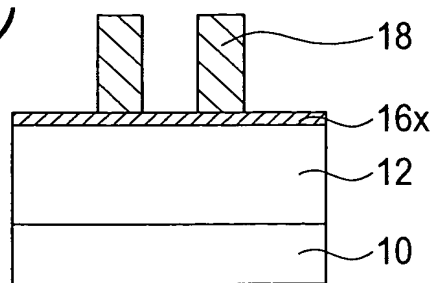


FIG. 11(B)

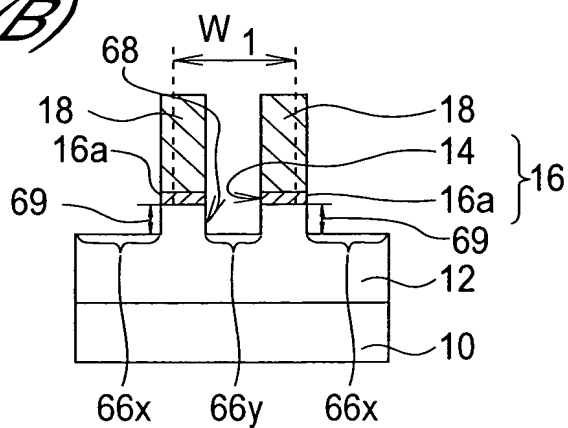


FIG. 11(C)

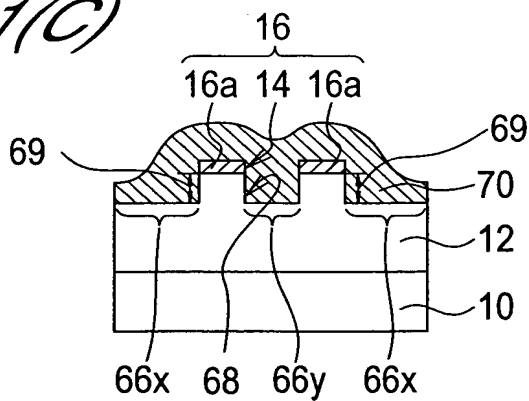
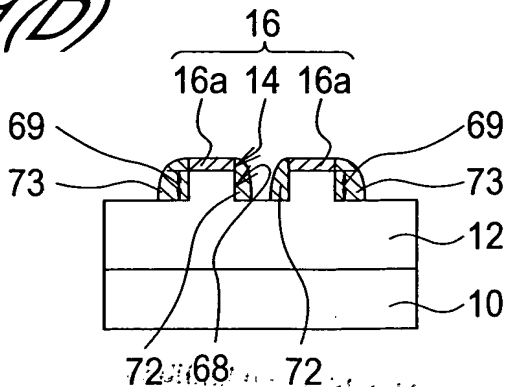


FIG. 11(D)



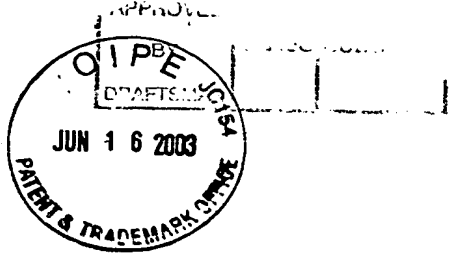


FIG. 12(A)

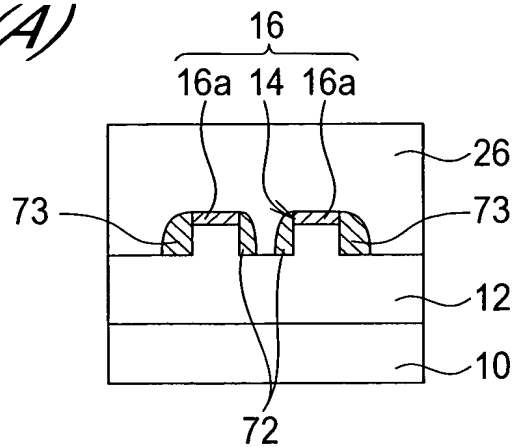


FIG. 12(B)

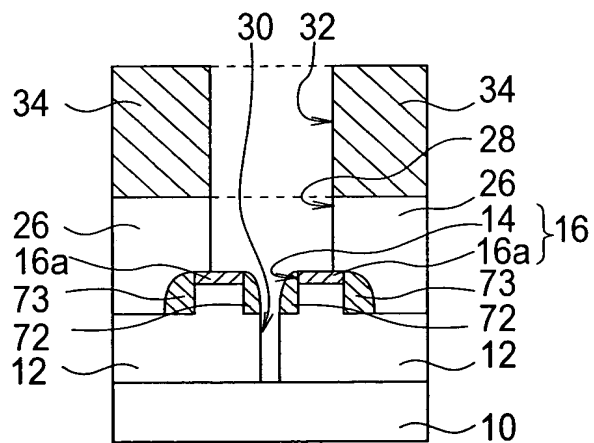
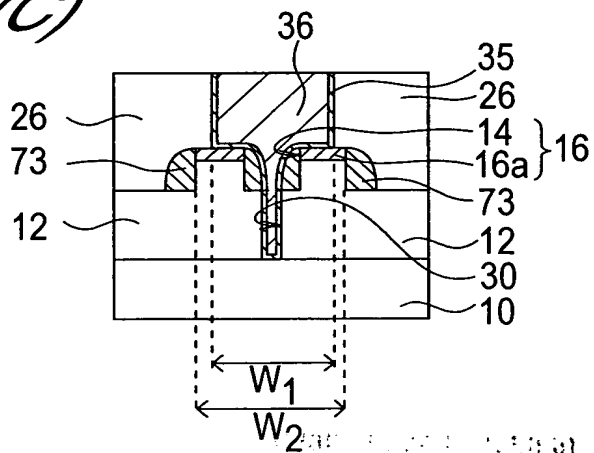


FIG. 12(C)



[illegible]

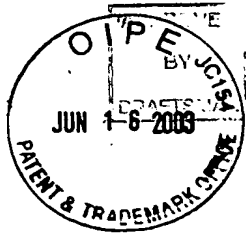


FIG. 14(A)

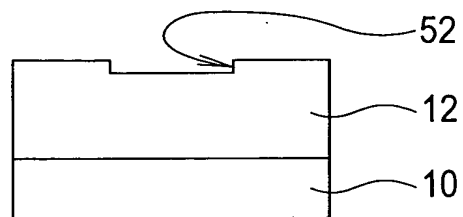


FIG. 14(B)

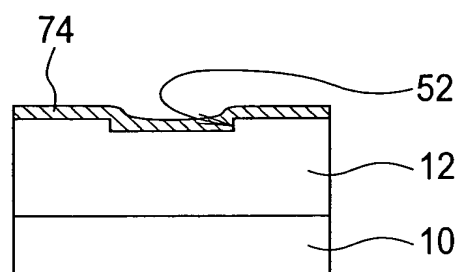


FIG. 14(C)

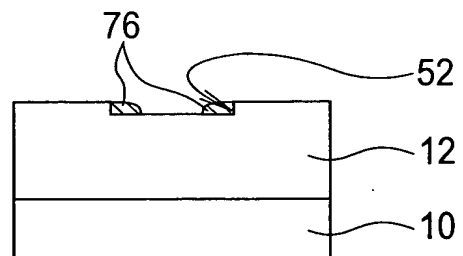


FIG. 14(D)

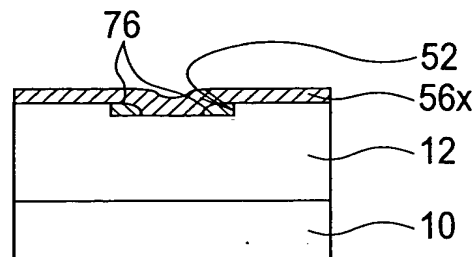




FIG. 15(A)

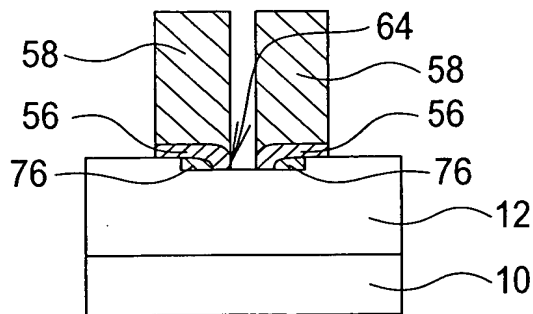


FIG. 15(B)

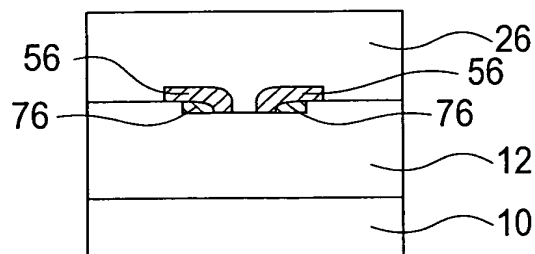


FIG. 15(C)

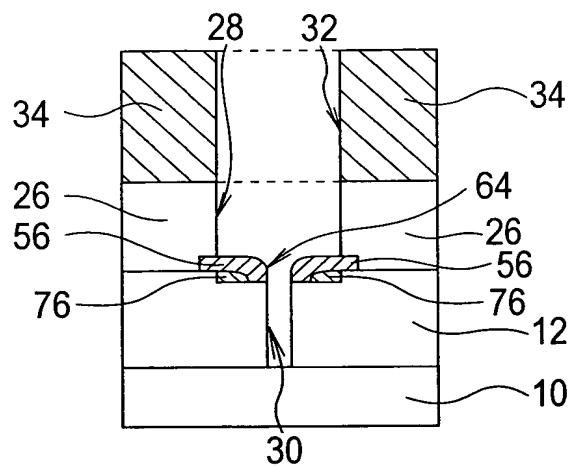


FIG. 15(D)

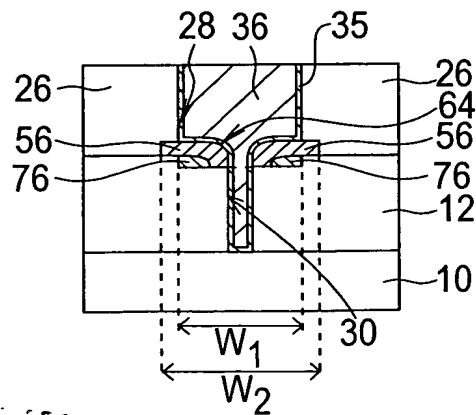




FIG. 16(A)

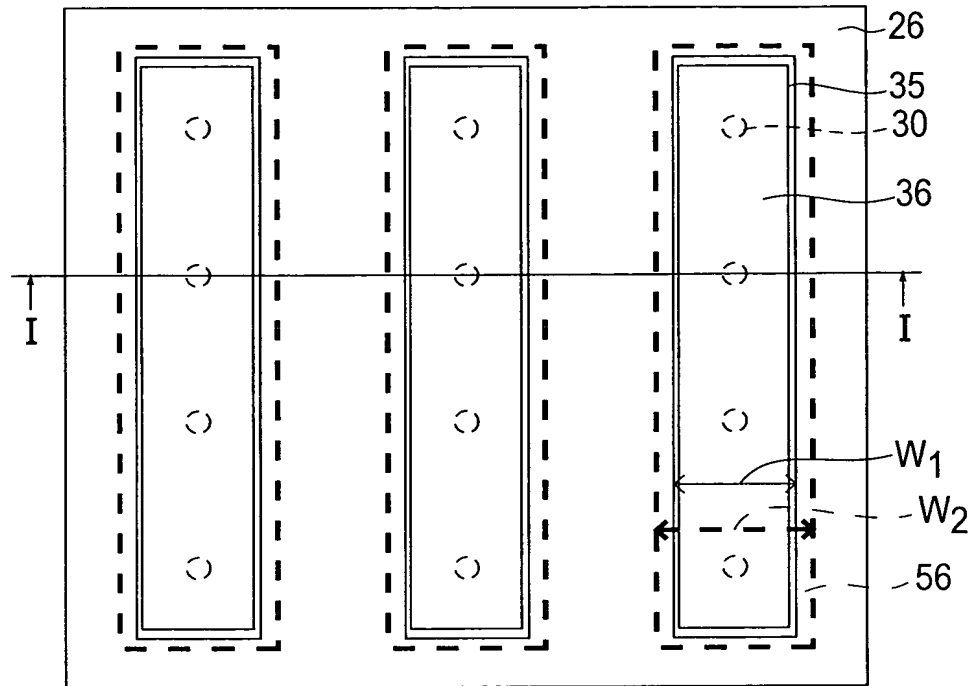


FIG. 16(B)

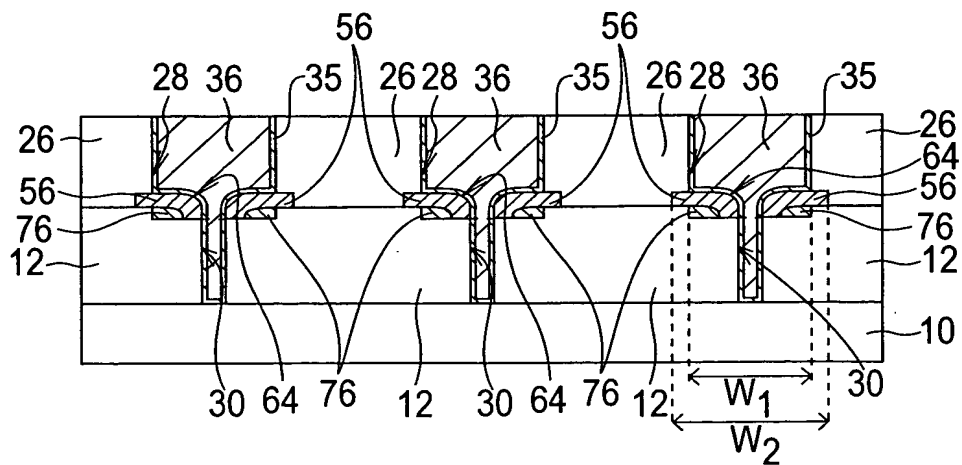




FIG. 17(A)

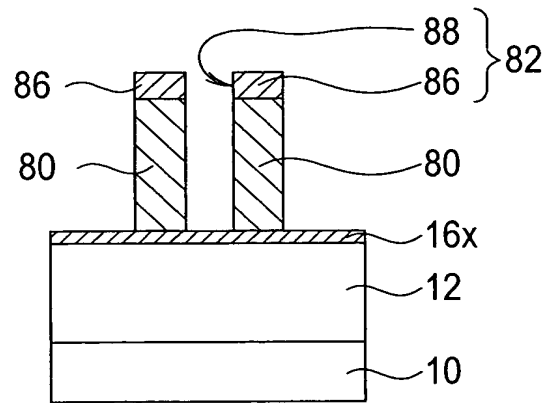


FIG. 17(B)

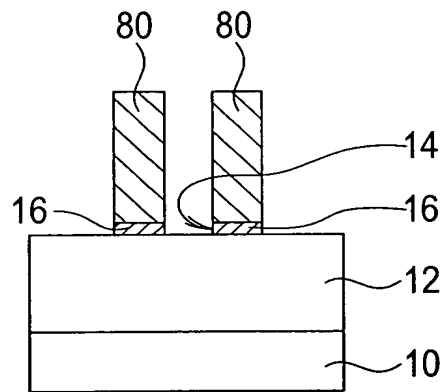
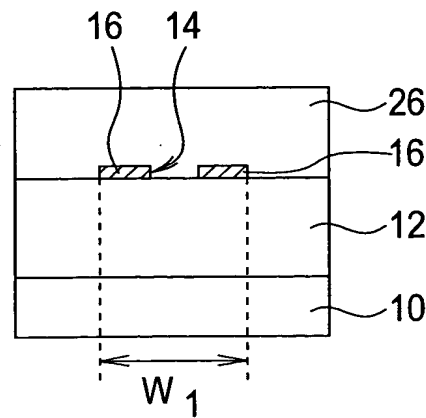


FIG. 17(C)



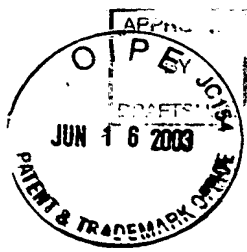


FIG. 18(A)

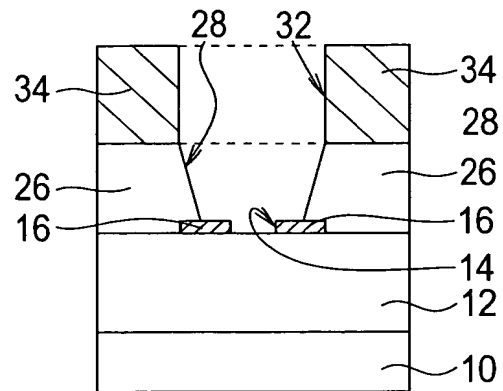


FIG. 18(B)

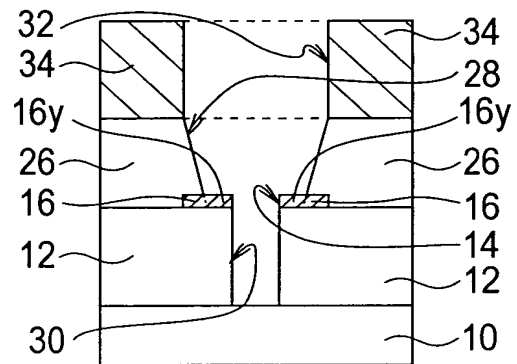


FIG. 18(C)

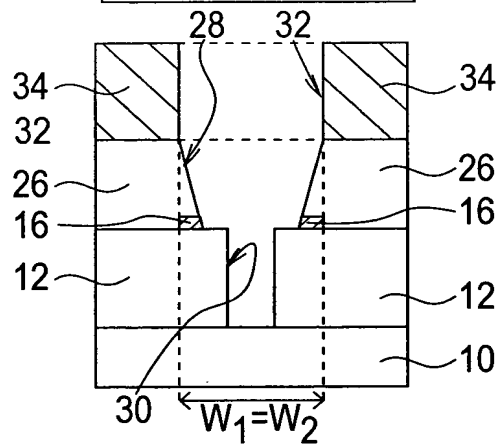


FIG. 18(D)

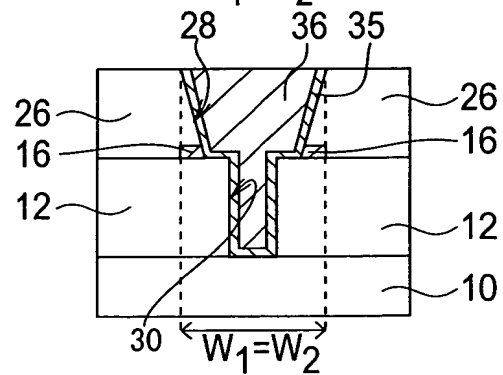




FIG. 19(A)

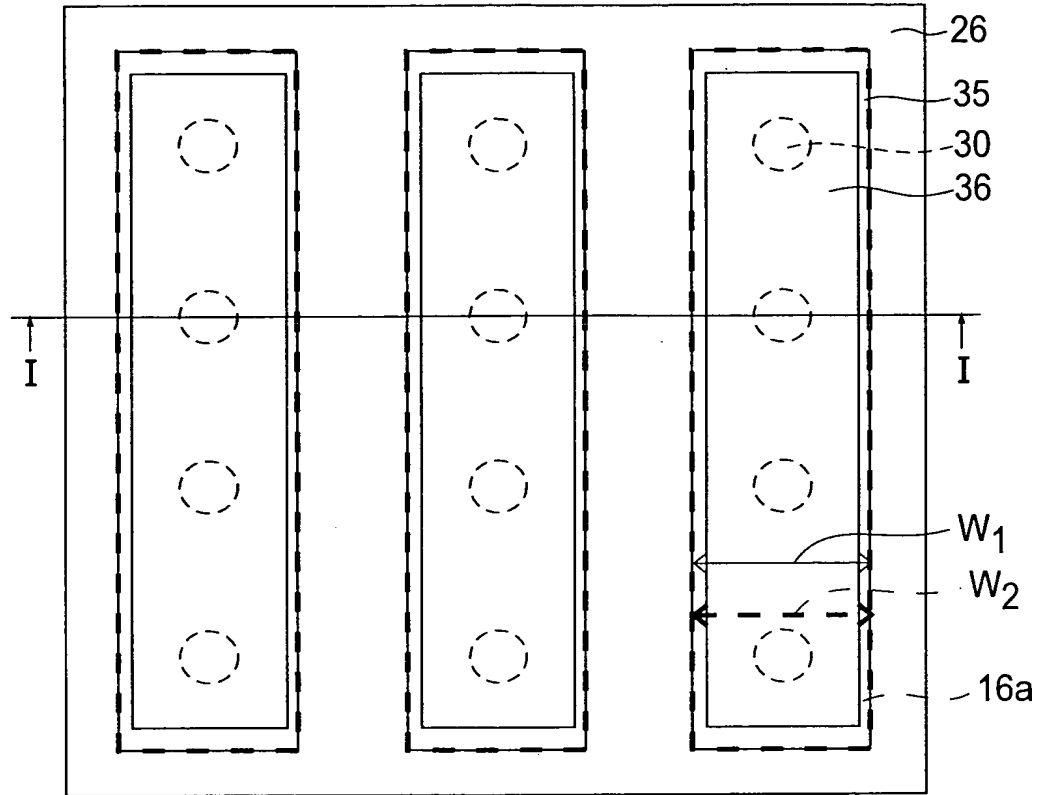


FIG. 19(B)

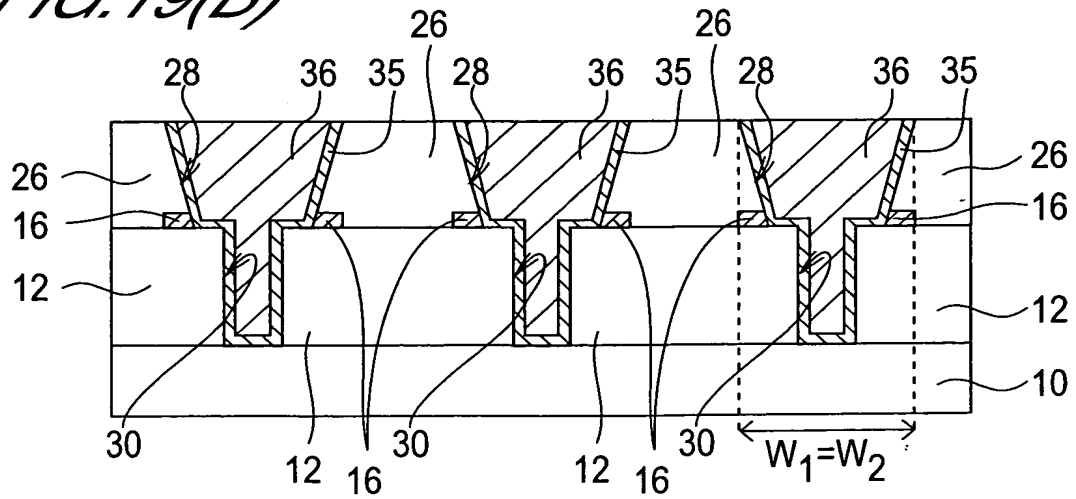




FIG. 20

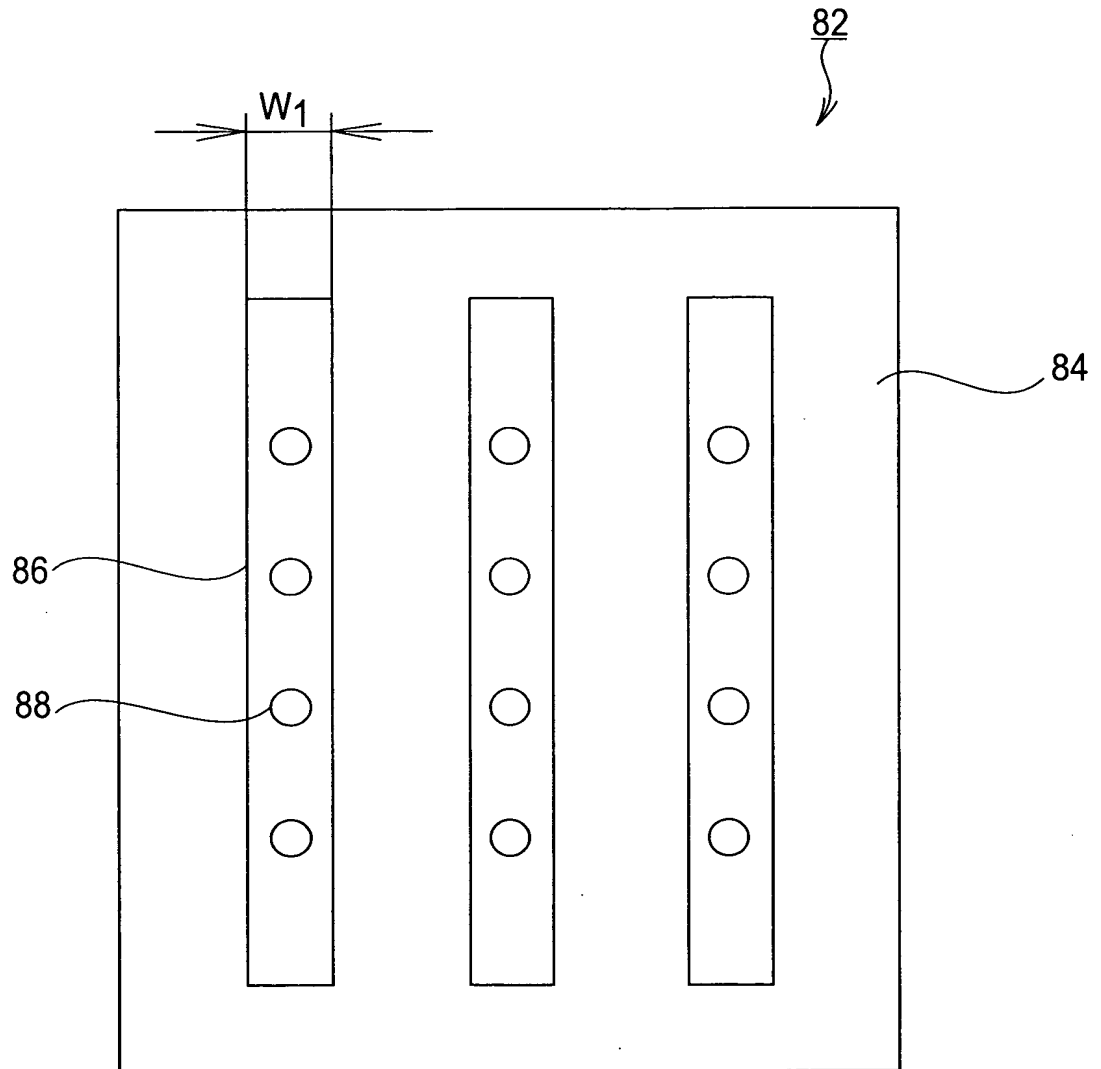


Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 10, a first layer 12, and a second layer 26. A central region 30 is defined by a dashed line. The first layer 12 has a width $W_1=W_2$. The second layer 26 has a width W_3 . The second layer 26 is divided into regions 37a and 37b. A central region 36 is defined by a dashed line. A layer 35 is shown on the right side of the device.

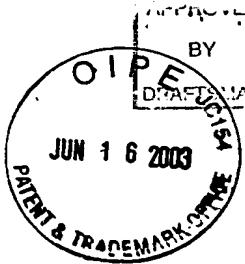


FIG.22(A)

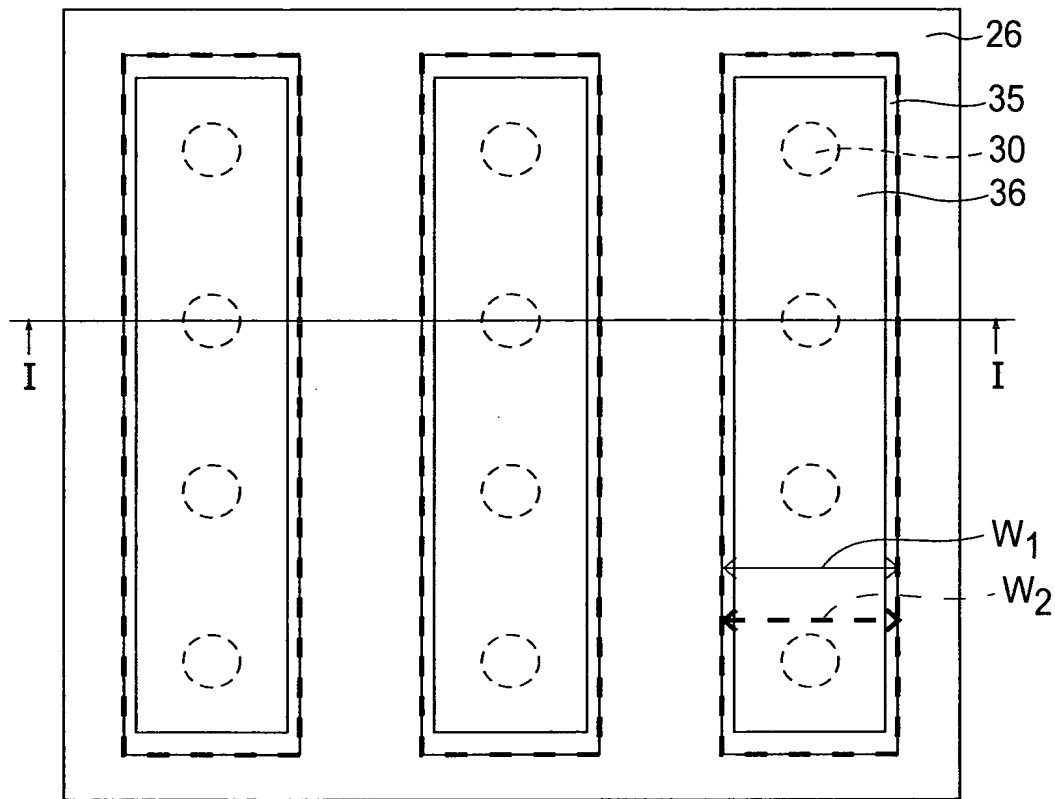


FIG.22(B)

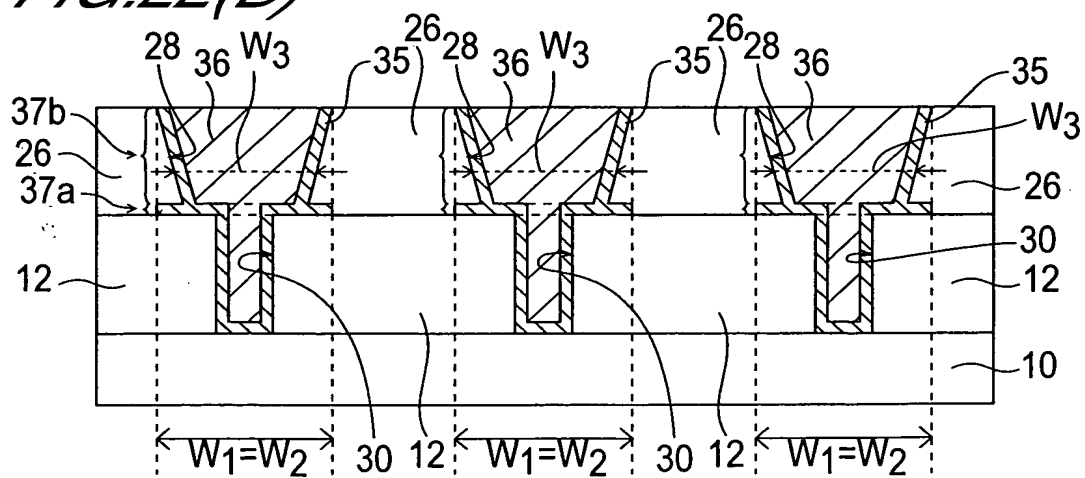




FIG.23(A)

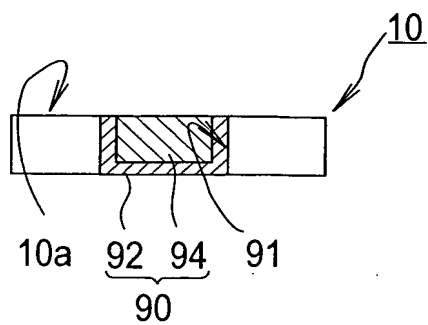


FIG.23(B)

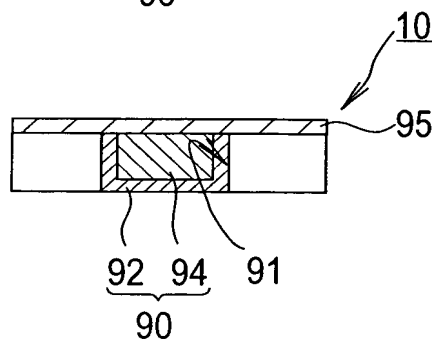


FIG.23(C)

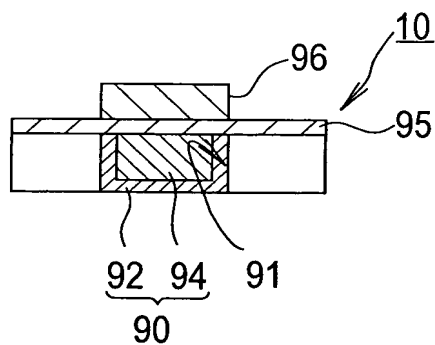


FIG.23(D)

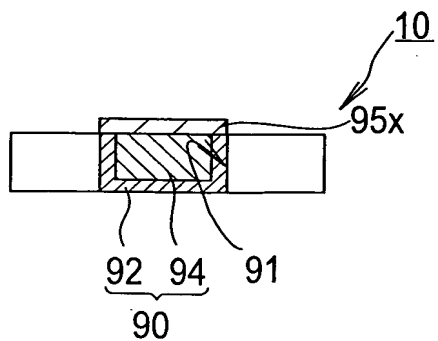




FIG.24(A)

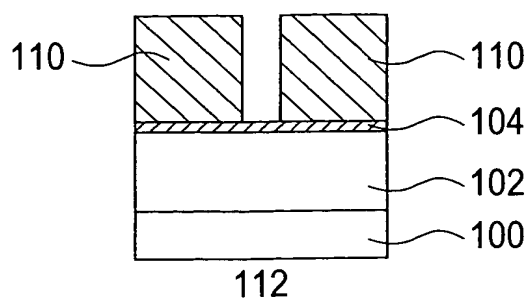


FIG.24(B)

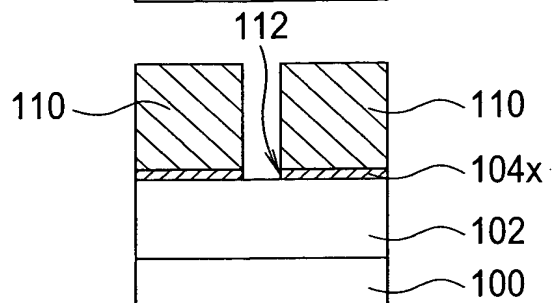


FIG.24(C)

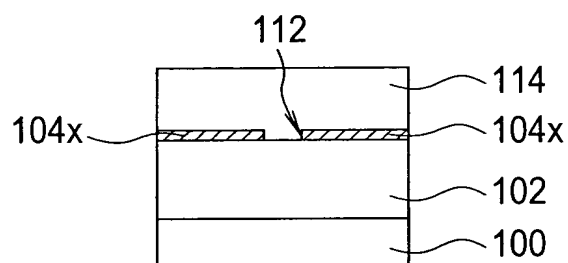


FIG.24(D)

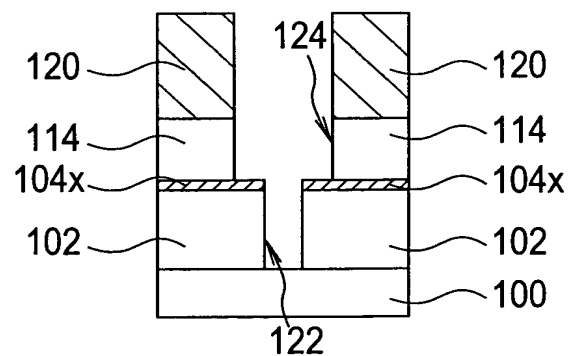


FIG.24(E)

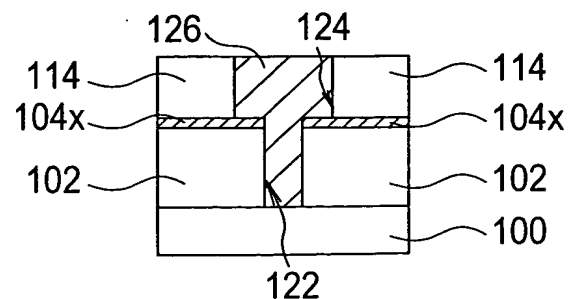




FIG.25

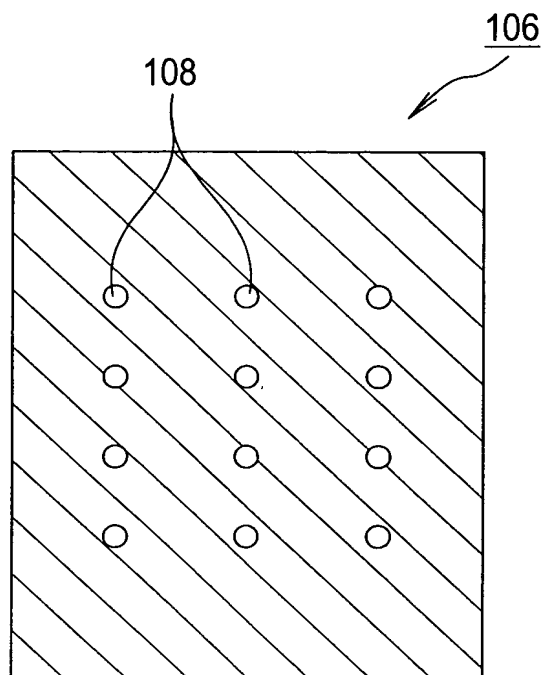
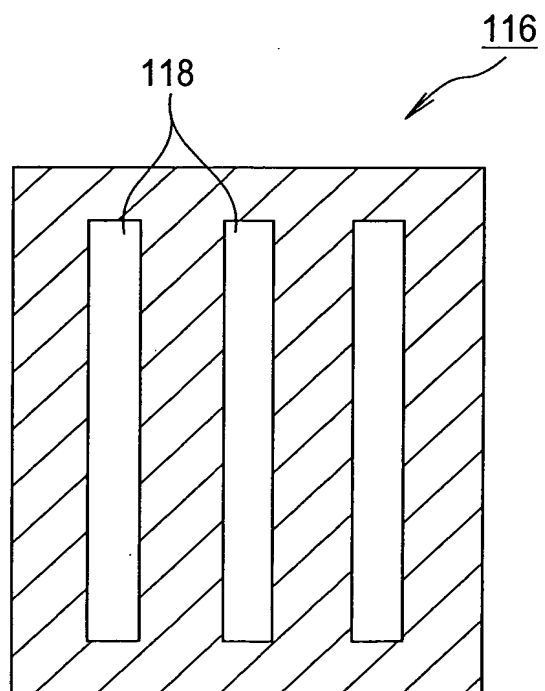


FIG.26



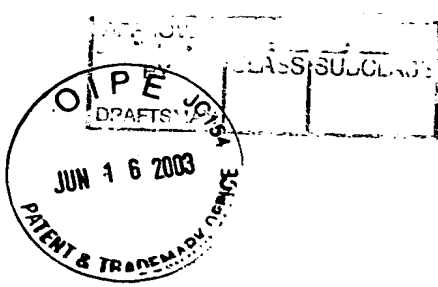


FIG. 27

